LH540235/45

ADVANCE INFORMATION

2K × 18 / 4K × 18 Synchronous FIFO

FEATURES

- Fast Cycle Times: 20/25/35 ns
- Pin-Compatible Drop-In Replacements for IDT72235B/45B FIFOs
- Choice of IDT-Compatible or ***Enhanced*** Operating Mode; Selected by an Input Control Signal
- Device Comes Up into One of Two Known Default States at Reset Depending on the State of the ***EMODE*** Control Input: Programming is Allowed, but is not Required
- Internal Memory Array Architecture Based on CMOS Dual-Port SRAM Technology, 1024 × 18 or 4046 × 18
- 'Synchronous' Enable-Plus-Clock Control at Both Input Port and Output Port
- Independently-Synchronized Operation of Input Port and Output Port
- Control Inputs Sampled on Rising Clock Edge
- Most Control Signals Assertive-LOW for Noise Immunity
- May be Cascaded for Increased Depth, or Paralleled for Increased Width
- 8 mA-IOL High-Drive Three-State Outputs With Built-In Series Resistor
- Five Status Flags: Full, Almost-Full, Half-Full, Almost-Empty, and Empty; 'Almost' Flags are Programmable
- ***In Enhanced Operating Mode, Almost-Full, Half-Full, and Almost-Empty Flags can be Made Completely Synchronous***
- ***In Enhanced Operating Mode, Duplicate Enables for Interlocked Paralleled FIFO Operation, for 36-Bit Data Width, when Selected and Appropriately Connected***
- ***In Enhanced Operating Mode, Disabling Three-State Outputs May be Made to Suppress Reading***
- ***Data Retransmit Function***
- TTL/CMOS-Compatible I/O
- Space-Saving 68-Pin PLCC and 64-Pin TQFP Packages

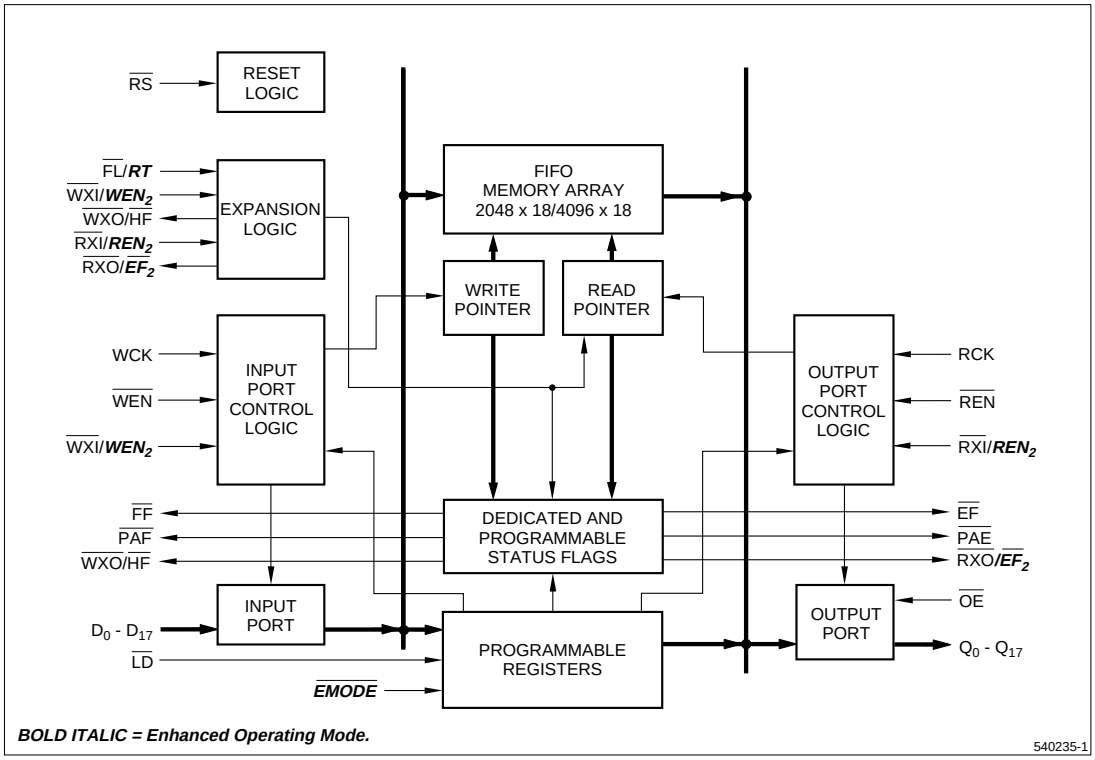

Figure 1. LH540235/45 Block Diagram

BOLD ITALIC = Enhanced Operating Mode

FUNCTIONAL DESCRIPTION

NOTE: Throughout this data sheet, a ***BOLD ITALIC*** type font is used for all references to ***Enhanced Operating Mode*** features which do not function in IDT-Compatible Operating Mode; and also for all references to the r***e-transmit*** facility (which is not an IDT72235B/45B FIFO feature), even though it may be used – subject to some restrictions – in either of these two operating modes. Thus, readers interested only in using the LH540235/45 FIFOs in IDT-Compatible Operating Mode may skip over ***BOLD ITALIC*** sections, if they wish.

The LH540235/45 are FIFO (First-In, First-Out) memory devices, based on fully-static CMOS dual-port SRAM technology, capable of containing up to 2K or 4K 18-bit words respectively. They can replace two or more byte-wide FIFOs in many applications, for microprocessor-to-microprocessor or microprocessor-to-bus communication. Their architecture supports synchronous operation, tied to two independent free-running clocks at the input and output ports respectively. However, these 'clocks' also may be aperiodic, asynchronous 'demand' signals. Almost all control-input signals and status-output signals are synchronized to these clocks, to simplify system design.

The input and output ports operate altogether independently of each other, unless the FIFO becomes either totally full or else totally empty. Data flow is initiated at a port by the rising edge of its corresponding clock, and is gated by the appropriate edge-sampled enable signals.

The following FIFO status flags monitor the extent to which the internal memory has been filled: Full, Almost-Full, Half-Full, Almost-Empty, and Empty. The Almost-Full and Almost-Empty flag offsets are programmable over the entire FIFO depth; but, during a reset operation, each of these is initialized to a default offset value of 63 (LH540235) or 127 (LH540245) FIFO-memory words, from the respective FIFO boundary. If this default offset value is satisfactory, no further programming is required.

After a reset operation during which the ***EMODE*** control input was not asserted (was HIGH), these FIFOs operate in the IDT-Compatible Operating Mode. In this mode, each part is pin-compatible and functionally-compatible with the IDT72235B/45B part of similar depth and speed grade; and the ***Control Register*** is not even accessible or visible to the external-system logic which is controlling the FIFO, although it still performs the same control functions.

However, assertion of the $\overline{EMODE}$ control input during a reset operation leaves Control Register bits 00-05 set, and causes the FIFO to operate in the Enhanced Operating Mode. In essence, asserting EMODE chooses a different default state for the Control Register. The system optionally then may program the Control Register in any desired manner to activate or deactivate any or all of the Enhanced-Operating-Mode features which it can control, including selectable-clock-edge flag synchronization, and read inhibition when the data outputs are disabled.

Whenever $\overline{EMODE}$ is being asserted, interlocked-operation paralleling also is available, by appropriate interconnection of the FIFO's expansion inputs.

The retransmit facility is available during standalone operation, in either IDT-Compatible Operating Mode or Enhanced Operating Mode. It is inoperative if the $\overline{FL}$/*RT* input signal is grounded. It is not an IDT72235B/45B feature. ***The Retransmit control signal causes the internal FIFO read-address pointer to be set back to zero, without affecting the internal FIFO write-address pointer. Thus, the Retransmit control signal also provides a mechanism whereby a block of data delimited by the zero physical address and the current write-address-pointer address may be read out repeatedly, an arbitrary number of times.***

The only restrictions are that neither the read-address pointer nor the write-address pointer may 'wrap around' during this entire process, and that the retransmit facility is not available during depth-cascaded operation, either in IDT-Compatible Operating Mode or in Enhanced Operating Mode. (See Tables 1 and 2.) Also, the flags behave differently for a short time after a retransmit operation. Otherwise, the retransmit facility is available during standalone operation, in either IDT-Compatible Operating Mode or Enhanced Operating Mode.

Note that, when $\overline{FL}$/RT is being used as RT, RT is an assertive-HIGH signal, rather than assertive-LOW as it is in most other FIFOs having a retransmit facility.

Programming the programmable-flag offsets, ***the timing synchronization of the various status flags, the optional read-suppression functionality of $\overline{OE}$***, and the behavior of the pointers which access the offset-value registers ***and the Control Register*** may be individually controlled by asserting the signal $\overline{LD}$, without any reset operation. When $\overline{LD}$ is being asserted, and writing is being enabled by asserting $\overline{WEN}$, some portion of the input bus word $D_0 – D_{17}$ is used at the next rising edge of WCLK to program one or more of the programmable registers on successive write clocks. Likewise, the values programmed into these programmable registers may be read out for verification by asserting $\overline{LD}$ and $\overline{REN}$, with the outputs $Q_0 – Q_{17}$ enabled. Reading out these programmable registers should not be initiated while they are being written into. Table 3 defines the possible modes of operation for loading and reading out the contents of programmable registers.

In the Enhanced Operating Mode, coordinated operation of two 18-bit FIFOs as one 36-bit FIFO may be ensured by 'interlocked' crosscoupling of the status-flag outputs from each FIFO to the expansion inputs of the other one; that is, $\overline{FF}$ to $\overline{WXI}$/$\overline{WEN_2}$, and $\overline{EF}$ to $\overline{RXI}$/$\overline{REN_2}$, in both directions between two paralleled FIFOs. This 'interlocked' operation takes effect automatically, if two paralleled FIFOs are crossconnected in this manner, with the $\overline{EMODE}$ control input being asserted (LOW). IDT-compatible depth cascading no longer is available when operating in this 'interlocked-paralleled' mode; however, pipelined depth cascading remains available.

BOLD ITALIC = Enhanced Operating Mode (features above and beyond IDT-Compatible Operating Mode).

PIN CONNECTIONS

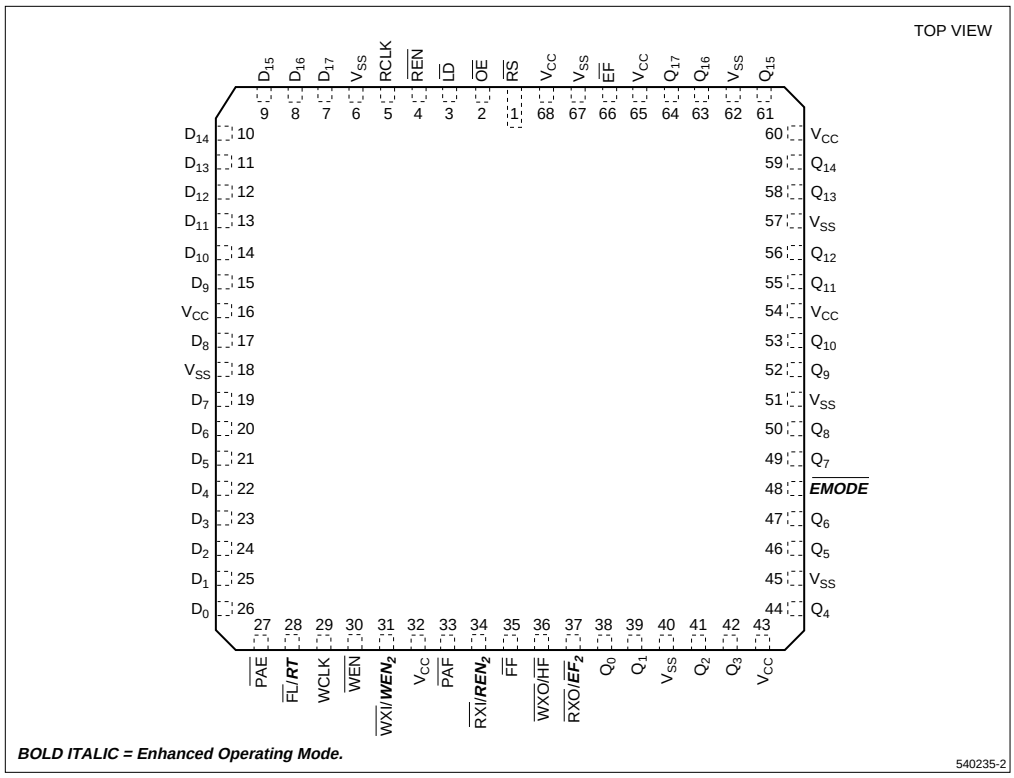

Figure 2. Pin Connections for 68-Pin PLCC Package

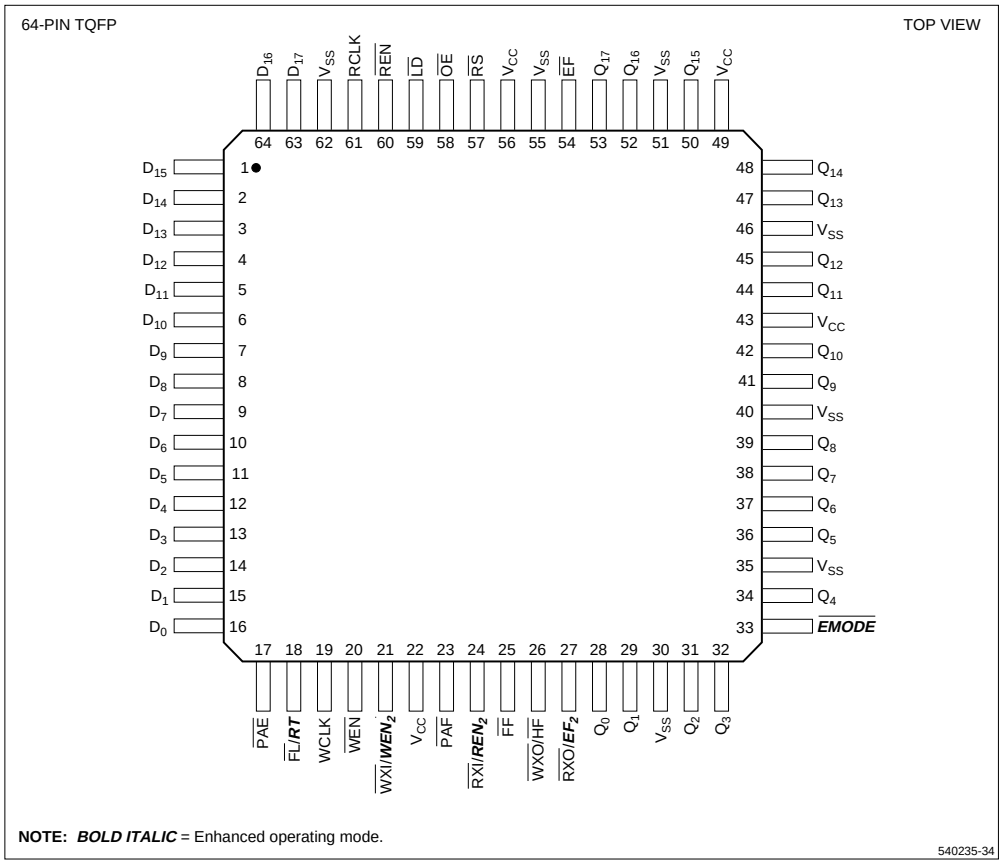

Figure 3. Pin Connections for TQFP Package